# Industrial Micro Systems Model 480

## Four Line Asynchronous Communication Controller

The Industrial Micro Systems Model 480 four line Asynchronous Communication Controller (ACC) interfaces four RS-232C line to the Series 5000 and 8000 IMS Systems.

The 480 requires 32 I/O address to transfer control and data information between the 480 Controller and CPU.

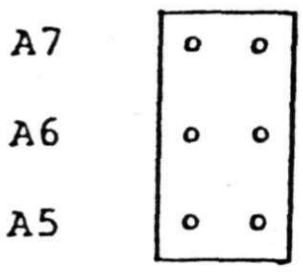
Control is accomplished by the Western Digital WD8250 Asynchronous Communication Element (ACE).

The Model 480 controller requires one slot in the S-100 bus. Each serial port is brought to a 3M 26 pin header. The RS-232-C ports are designed as Data Terminal Equipment (DTE) to connect directly to modems. To connect to terminals the RS-232 cable wires must be scrambled for Terminal to Terminal connection.

# Model 480 All Board

## Shunt and Jumper Options

JA



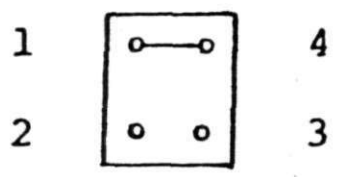

### I/O Address Select

Shunt off = 1  Shunt on = 0

(all Shunt off = I/O Address E0 - $FF_{16}$)

(all Shunt on = I/O Address 00 - $1F_{16}$)

JB




### Clock Option

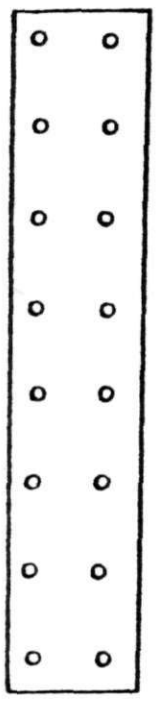
Etch jumper at JB = External 2MHZ

To change for internal clock for Baud Rates

cut jumper JB 1-2 Add jumper JB 2-4

add Osc at 15C and 74LS161 at 14C

### Interrupt Options




The installing of a shunt will attach the selected interrupt level to the line as defined below:

JC - ACC line 0

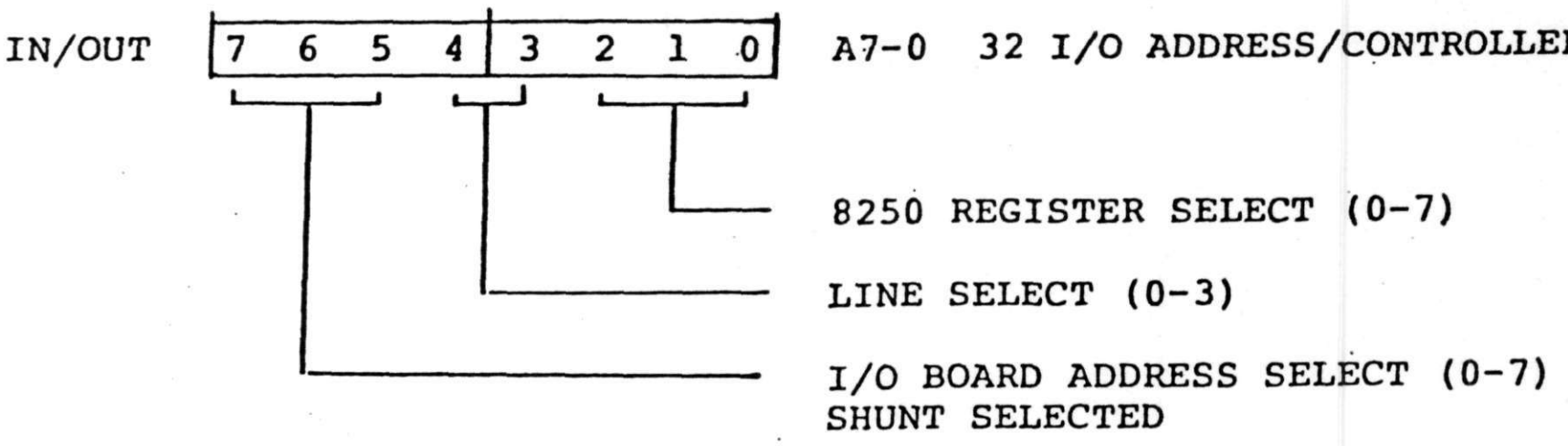
JD - ACC line 1

JE - ACC line 2

JF - ACC line 3

JC - JF

## 480 4-LINE COMMUNICATION CONTROLLER



# 480 Serial Port to RS-232 Connector

| Signal Name | RS-232C Circuit Name | J(X) Connector Pin Number | | DTE RS-232C Connector Pin Number |
|---|---|---|---|---|
| Transmit Data (Data to Modem) | BA | 3 | _____ | 2 |
| Receive Data (Data from Modem) | BB | 5 | _____ | 3 |
| Request to Send | CA | 7 | _____ | 4 |
| Clear to Send | CB | 9 | _____ | 5 |
| Data Set Ready | CC | 11 | _____ | 6 |
| Signal Ground | AB | 13 | _____ | 7 |
| Data Terminal Ready | CD | 14 | _____ | 20 |
| Data Carrier Detect | CF | 15 | _____ | 8 |
| Ring Indicator | CE | 18 | _____ | 22 |

( 26 conductor )
( 3M ribbon cable)

| | |
|---|---|
| 3M Socket | DB-25S |
| 3399-6000 | 3M-3483-1000 |
| | AMP 206770-1 |

WESTERN DIGITAL
CORPORATION

# WD8250 Asynchronous Communications Element

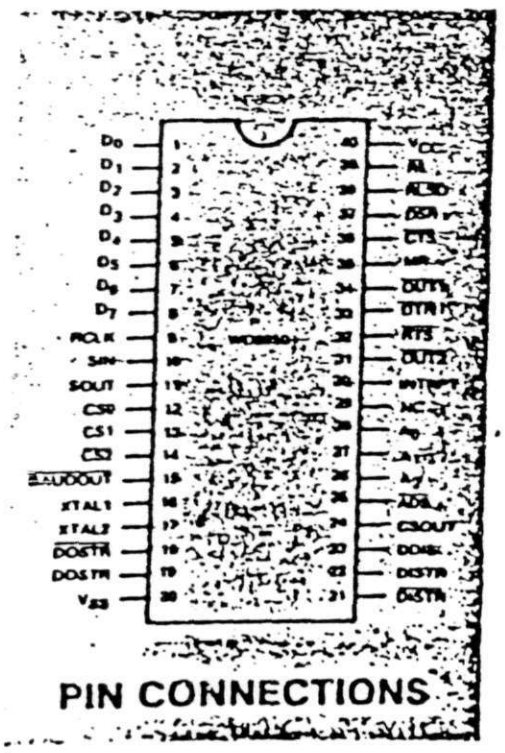
## FEATURES

- Designed to be Easily Interfaced to Most Popular Microprocessors (Z-80, 8080A, 6800, etc.)
- Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop, and Parity) to or from Serial Data Stream
- Full Double Buffering Eliminates Need for Precise Synchronization
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Programmable Baud Rate Generator Allows Division of Any Input Clock by 1 to ($2^{16}$ – 1) and Generates the Internal 16x Clock
- Independent Receiver Clock Input
- Fully Programmable Serial-Interface Characteristics
  - — 5-, 6-, 7-, or 8-Bit Characters
  - — Even, Odd, or No-Parity Bit Generation and Detection
  - — 1-, 1½-, or 2-Stop Bit Generation
  - — Baud Rate Generation (DC to 56K Baud)
- False Start Bit Detector
- Complete Status Reporting Capabilities
- THREE-STATE TTL Drive Capabilities for Bidirectional Data Bus and Control Bus
- Line Break Generation and Detection
- Internal Diagnostic Capabilities
  - — Loopback Controls for Communications Link Fault Isolation
  - — Break, Parity, Overrun, Framing Error Simulation
- Full Prioritized Interrupt System Controls
- Single +5-Volt Power Supply

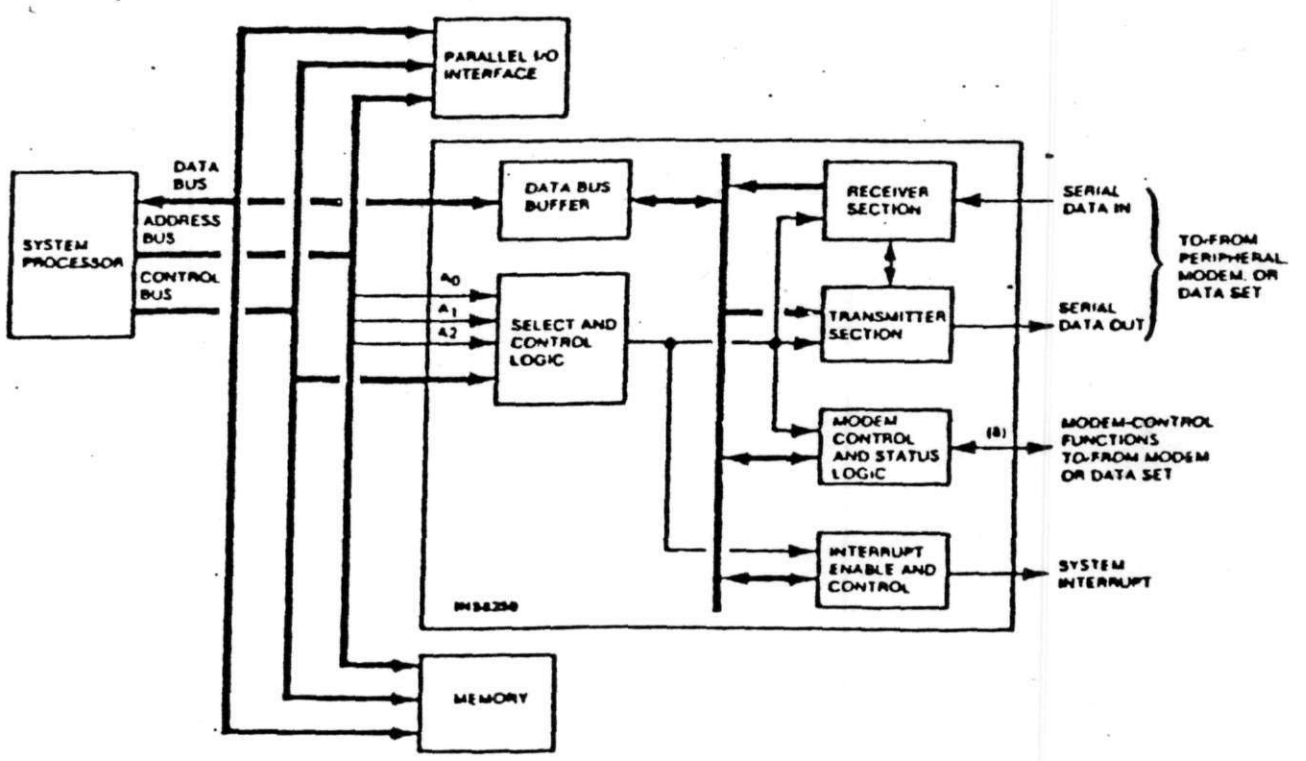
## GENERAL DESCRIPTION

The WD8250 is a programmable Asynchronous Communications (ACE) chip contained in a standard 40-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate technology, functions as a seial data input/output interface in a microcomputer system. The functional configuration of the WD8250 is programmed by the system software via a THREE-STATE 8-bit bidirectional data bus.

The WD8250 performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the WD8250 at any time during the functional operation. Status information reported includes the type and condition of the transfer opertions being performed by the WD8250, as well as any error conditions (parity, overrun, framing, or break interrupt).




PIN CONNECTIONS




WD8250 GENERAL SYSTEM CONFIGURATION

In addition to providing control of asynchronous data communications, the WD8250 includes a programmable Baud Generator that is capable of dividing the timing reference clock input by divisors of 1 to ($2^{16} - 1$), and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the WD8250 is a complete MODEM-control capability, and a processor-interrupt system that may be software tailored to the user's requirements to minimize the computing time required to handle the communications link.

## WD8250 FUNCTIONAL PIN DESCRIPTION

The following describes the function of all WD8250 input/output pins. Some of these descriptions reference internal circuits.

NOTE

In the following descriptions, a low represents a logic 0 (0 volt nominal) and a high represents a logic 1 (+2.4 volts nominal).

### Input Signals

**Chip Select (CS0, CS1, $\overline{CS2}$), Pins 12-14:** When CS0 and CS1 are high and $\overline{CS2}$ is low, the chip is selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) Address Strobe ($\overline{ADS}$) input. This enables communication between the WD8250 and the CPU.

**Data Input Strobe (DISTR, $\overline{DISTR}$), Pins 22 and 21:** When DISTR is high or $\overline{DISTR}$ is low while the chip is selected, allows the CPU to read status information or data from a selected register of the WD8250.

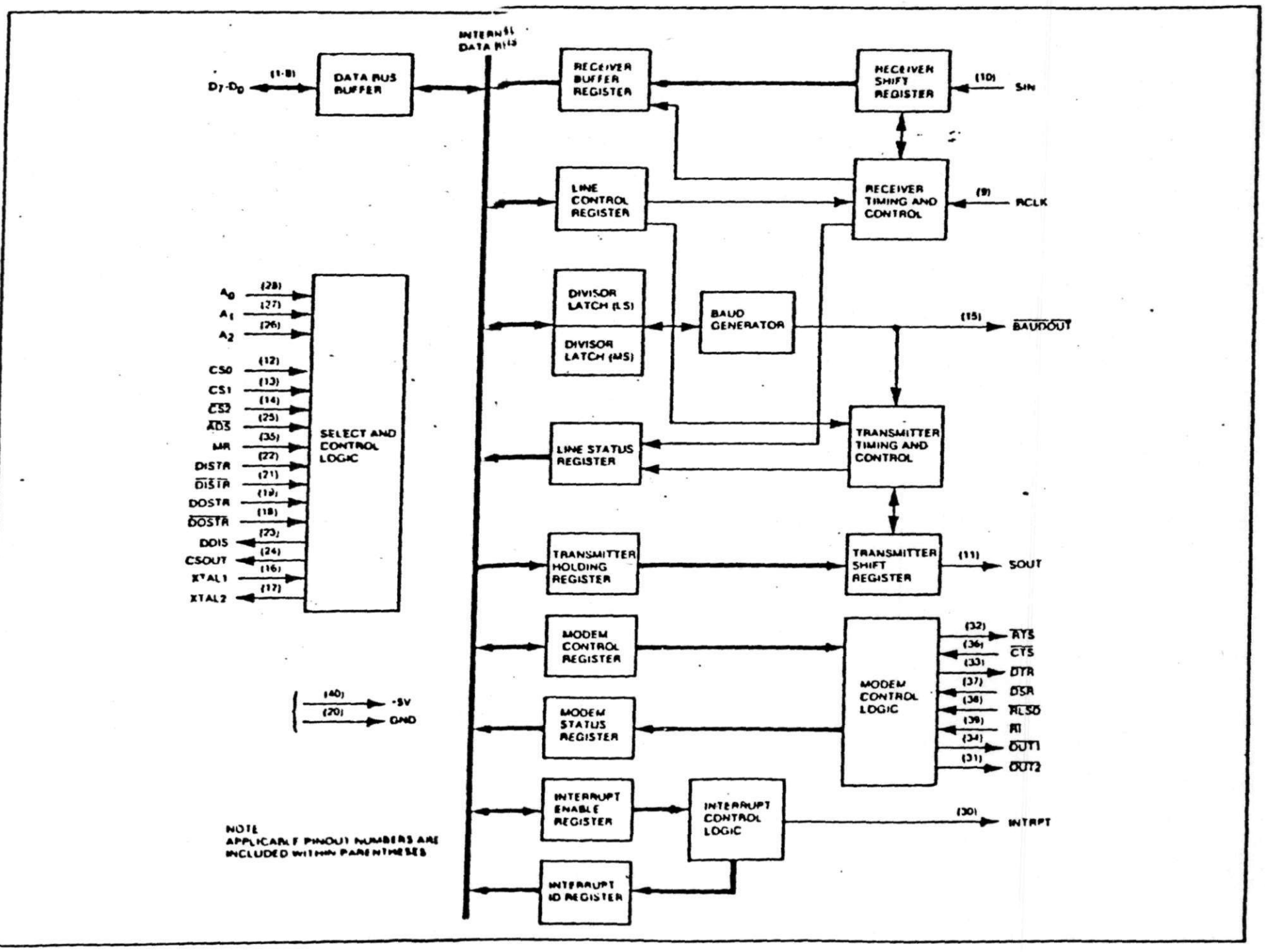
NOTE

Only an active DISTR or $\overline{DISTR}$ input is required to transfer data from the WD8250 during a read operation. Therefore, tie either the DISTR input permanently low or the $\overline{DISTR}$ input permanently high, if not used.

**Data Output Strobe (DOSTR, $\overline{DOSTR}$), Pins 19 and 18:** When DOSTR is high or $\overline{DOSTR}$ is low while the chip is selected, allows the CPU to write data or control words into a selected register of the WD8250.

NOTE

Only an active DOSTR or $\overline{DOSTR}$ input is required to transfer data to the WD8250 during a write operation. Therefore, tie either the DOSTR input permanently low or the $\overline{DOSTR}$ input permanently high, if not used.




**WD8250 BLOCK DIAGRAM**

**Address Stobe ($\overline{ADS}$), Pin 25:** When low, provides latching for the Register Select (A0, A1, A2) and Chip Select (CS0 CS1, $\overline{CS2}$) signals.

NOTE

An active $\overline{ADS}$ input is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the $\overline{ADS}$ input permanently low.

**Register Select (A0, A1, A2), Pins 26-28:** These three inputs are used during a read or write operation to select a WD8250 register to read from or write into as indicated in the table below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain WD8250 registers. The DLAB is reset low when the Master Reset (MR) input is active (low); the DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

| DLAB | A2 | A1 | A0 | Register |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Receiver Buffer (read), Transmitter Holding Register (write) |
| 0 | 0 | 0 | 1 | Interrupt Enable |
| X | 0 | 1 | 0 | Interrupt Identification (read only) |
| X | 0 | 1 | 1 | Line Control |
| X | 1 | 0 | 0 | MODEM Control |
| X | 1 | 0 | 1 | Line Status |
| X | 1 | 1 | 0 | MODEM Status |
| X | 1 | 1 | 1 | None |
| 1 | 0 | 0 | 0 | Divisor Latch (least significant byte) |
| 1 | 0 | 0 | 1 | Divisor Latch (most significant byte) |

**Master Reset (MR), Pin 35:** When high, clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the WD8250. Also, the state of various output signals (SOUT, INTRPT, $\overline{OUT1}$, $\overline{OUT2}$, $\overline{RTS}$, $\overline{DTR}$) are affected by an active MR input. (Refer to table 1.)

**Receiver Clock (RCLK), Pin 9:** This input is the 16x baud rate clock for the receiver section of the chip.

**Serial Input (SIN), Pin 10:** Serial data input from the communications link (peripheral device, MODEM, or data set).

**Clear to Send ($\overline{CTS}$), Pin 36:** The $\overline{CTS}$ signal is a MODEM control function input whose condition can be tested by the CPU by reading bit 4 (CTS) of the MODEM Status Register. Bit 0 (DCTS) of the MODEM Status Register indicates whether the $\overline{CTS}$ input has changed state since the previous reading of the MODEM Status Register.

NOTE

Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if enabled.

**Data Set Ready ($\overline{DSR}$), Pin 37:** When low, indicates that the MODEM or data set is ready to establish the communications link and transfer data with the WD8250. The $\overline{DSR}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 5 (DSR) of the MODEM Status Register. Bit 1 (DDSR) of the MODEM Status Register indicates whether the $\overline{DSR}$ input has changed state since the previous reading of the MODEM Status Register.

NOTE

Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if enabled.

**Received Line Signal Detect ($\overline{RLSD}$), Pin 38:** When low, indicates that the data carrier has been detected by the MODEM or data set. The $\overline{RLSD}$ signal is a MODEM-control function input whose conditin can be tested by the CPU by reading bit 7 (RLSD) of the MODEM Status Register. Bit 3 (DRLSD) of the MODEM Status Register indicates whether the $\overline{RLSD}$ input has changed state since the previous reading of the MODEM Status Register.

NOTE

Whenever the RLSD bit of the MODEM Status Register changes state, an interrupt is generated if enabled.

**Ring Indicator ($\overline{RI}$), Pin 39:** When low, indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM-control function input whose condition can be tested CPU by reading bit 6 (RI) of the MODEM Status Register. Bit 2 (TERI) of the MODEM Status Register indicates whether the $\overline{RI}$ input has changed from a low to a high state since the previous reading of the MODEM Status Register.

NOTE

Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if enabled.

**VCC, Pin 40:** +5-volt supply.

**VSS, Pin 20:** Ground (0-volt) reference.

**Output Signals**

**Data Terminal Ready ($\overline{DTR}$), Pin 33:** When low, informs the MODEM or data set that the WD8250 is ready to communicate. The DTR output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. The $\overline{DTR}$ signal is set high upon a Master Reset operation.

**Request to Send ($\overline{RTS}$), Pin 32:** When low, informs the MODEM or data set that the WD8250 is ready to transmit data. The $\overline{RTS}$ output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. The $\overline{RTS}$ signal is set high upon a Master Reset operation.

**Output 1 ($\overline{OUT\ 1}$), Pin 34:** User-designated output that can be set to an active low by programming bit 2 ($\overline{OUT\ 1}$) of the MODEM Control Register to a high level. The $\overline{OUT\ 1}$ signal is set high upon a Master Reset operation.

**Output 2 ($\overline{OUT\ 2}$), Pin 31:** User-designated output that can be set to an active low by programming bit 3 ($\overline{OUT\ 2}$) of the MODEM Control Register to a high level. The $\overline{OUT\ 2}$ signal is set high upon a Master Reset operation.

**Chip Select Out (CSOUT), Pin 24:** When high, indicates that the chip has been selected by active CS0, CS1, and $\overline{CS2}$ inputs. No data transfer can be initiated until the CSOUT signal is a logic 1.

**Driver Disable (DDIS), Pin 23:** Goes low whenever the CPU is reading data from the WD8250. A high-level DDIS output can be used to disable an external transceiver (if used between the CPU and WD8250 on the $D_7$-$D_0$ Data Bus) at all times, except when the CPU is reading data.

**Baud Out ($\overline{BAUDOUT}$), Pin 15:** 16x clock signal for the transmitter section of the WD8250. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input of the chip.

**Interrupt (INTRPT), Pin 30:** Goes high whenever any one of the following interrupt sources has an active high condition: Receiver Error Flag; Received Data Available; Transmitter Holding Register Empty; and MODEM Status. The INTRPT signal is reset low upon a Master Reset operation.

**Serial Output (SOUT), Pin 11:** Composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset Operation.

### Input/Output Signals

**Data ($D_7$-$D_0$) Bus, Pins 1-8:** This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communications between the WD8250 and the CPU. Data, control words, and status information are transferred via the $D_7$-$D_0$ Data Bus.

**External Clock Input/Output (XTAL 1, XTAL 2), Pins 16 and 17:** These two pins connect the main timing reference (crystal or signal clock) to the WD8250.

**Table 1. Reset Control of Registers and Pinout Signals**

| Register/Signal | Reset Control | Reset State |
|---|---|---|
| Receiver Buffer Register | First Word Received | Data |
| Transmitter Holding Register | Writing into the Transmitter Holding Register | Data |
| Interrupt Enable Register | Master Reset | All Bits Low (0-3 forced and 4-7 permanent) |
| Interrupt Identification Register | Master Reset | Bit 0 is High and Bits 1-7 Are Permanently Low |
| Line Control Register | Master Reset | All Bits Low |
| MODEM Control Register | Master Reset | All Bits Low |
| Line Status Register | Master Reset | All Bits Low, Except Bits 5 and 6 Are High |
| Modem Status Register | Master Reset MODEM Signal Inputs | Bits 0-3 Low Bits 4-7 — Input Signal |
| Divisor Latch (low order bits) | Writing into the Latch | Data |
| Divisor Latch (high order bits) | Writing into the Latch | Data |
| SOUT | Master Reset | High |
| $\overline{BAUDOUT}$ | Writing into either Divisor Latch | Low |
| CSOUT | $\overline{ADS}$ Strobe Signal and State of Chip Select Lines | High/Low |
| DDIS | DDIS = $\overline{CSOUT}$ • RCLK • DISTR (At Master Reset the CPU sets RCLK and DISTR low.) | High |
| INTRPT | Master Reset | Low |
| $\overline{OUT\ 2}$ | Master Reset | High |
| $\overline{RTS}$ | Master Reset | High |
| $\overline{DTR}$ | Master Reset | High |
| $\overline{OUT\ 1}$ | Master Reset | High |
| D7-D0 Data Bus Lines | In THREE-STATE Mode, Unless CSOUT • DISTR = High or CSOUT • DOSTR = High | THREE-STATE Data (ACE to CPU) Data (CPU to ACE) |

## WD8250 ACCESSIBLE REGISTERS

The system programmer may access or control any of the WD8250 registers summarized in table 2 via the CPU. These registers ae used to control WD8250 operations and to transmit and receive data.

### WD8250 Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the Line Control Register are indicated and are described below.

**Table 2. Summary of WD8250 Accessible Registers**

| | Register Address | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 0 DLAB=0 | 0 DLAB=0 | 1DLAB=0 | 2 | 3 | 4 | 5 | 6 | 0DLAB=1 | 1DLAB=1 |
| Bit No. | Receiver Buffer Register (Read Only) | Holding Register (Write Only) | Interrupt Enable Register | Interrupt Identification Register | Line Control Register | MODEM Control Register | Line Status Register | MODEM Status Register | Divisor Latch (LS) | Divisor Latch (MS) |
| 0 | Data Bit 0* | Data Bit 0 | Enable Received Data Available Interrupt (ERBFI) | "0" if Interrupt Pending | Word Length Select Bit 0 (WLS0) | Data Terminal Ready (DTR) | Data Ready (DR) | Delta Clear to Send (DCTS) | Bit 0 | Bit 8 |
| 1 | Data Bit 1 | Data Bit 1 | Enable Transmitter Holding Register Empty Interrupt (ETBEI) | Interrupt ID Bit (0) | Word Length Select Bit 1 WLS1) | Request to Send (RTS) | Overrun Error (OR) | Delta Data Set Ready (DDSR) | Bit 1 | Bit 9 |
| 2 | Data Bit 2 | Data Bit 2 | Enable Receiver Line Status Interrupt (ELSI) | Interrupt ID Bit (1) | Number of Stop Bits (STB) | Out 1 | Parity Error (PE) | Trailing Edge Ring Indicator (TERI) | Bit 2 | Bit 10 |
| 3 | Data Bit 3 | Data Bit 3 | Enable MODEM Status Interrupt (EDSSI) | 0 | Parity Enable (PEN) | Out 2 | Framing Error (FE) | Delta Receive Line Signal Detect (DSLSD) | Bit 3 | Bit 11 |
| 4 | Data Bit 4 | Data Bit 4 | 0 | 0 | Even Parity Select (EPS) | Loop | Break Interrupt (BI) | Clear to Send (CTS) | Bit 4 | Bit 12 |
| 5 | Data Bit 5 | Data Bit 5 | 0 | 0 | Stick Parity | 0 | Transmitter Holding Register Empty (THRE) | Data Set Ready (DSR) | Bit 5 | Bit 13 |
| 6 | Data Bit 6 | Data Bit 6 | 0 | 0 | Set Break | 0 | Transmitter Shift Register Empty (TSRE) | Ring Indicator (RI) | Bit 6 | Bit 14 |
| 7 | Data Bit 7 | Data Bit 7 | 0 | 0 | Divisor Latch Access Bit (DLAB) | 0 | 0 | Received Line Signal Detect (RLSD) | Bit 7 | Bit 15 |

*Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

| Bit 1 | Bit 0 | Word Length |
|---|---|---|
| 0 | 0 | 5 Bits |
| 0 | 1 | 6 Bits |
| 1 | 0 | 7 Bits |
| 1 | 1 | 8 Bits |

Bit 2: This bit specifies the number of stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1½ Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there (until reset by a low-lever bit 6) regardless of other transmitter activity. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

### WD8250 Programmable Baud Rate Generator

The WD8250 contains a programmable Baud Rate Generator that is capable of taking any clock input (DC to 3.1 MHz) and dividing it by any divisor from 1 to ($2^{16}$ - 1). The output frequency of the Baud Generator is 16x the Baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3 and 4 illustrate the use of the Baud Generator with two different driving frequencies. One is referenced to a 1.8432 MHz crystal. The other is a 3.072 MHz crystal.

NOTE

The maximum operating frequency of the Baud Generator is 3.1 MHz. However, when using divisors of 5 and below, the maximum frequency is equal to the divisor in MHz. For example, if the divisor is 1, then the maximum frequency is 1 MHz. In no case should the data rate be greater than 56K Baud.

**Table 3. Baud Rates Using 1.8432 MHz Crystal.**

| Desired Baud Rate | Divisor Used to Generate 16x Clock | Percent Error Difference Between Desired and Actual |
|---|---|---|
| 50 | 2304 | — |
| 75 | 1536 | — |
| 110 | 1047 | 0.026 |
| 134.5 | 857 | 0.058 |
| 150 | 768 | — |
| 300 | 384 | — |
| 600 | 192 | — |
| 1200 | 96 | — |
| 1800 | 64 | — |
| 2000 | 58 | 0.69 |
| 2400 | 48 | — |
| 3600 | 32 | — |
| 4800 | 24 | — |
| 7200 | 16 | — |
| 9600 | 12 | — |
| 19200 | 6 | — |
| 38400 | 3 | — |
| 56000 | 2 | 2.86 |

NOTE: 1.8432 MHz is the standard 8080 frequency divided by 10.

**Table 4. Baud Rates Using 3.072 MHz Crystal.**

| Desired Baud Rate | Divisor Used to Generate 16x Clock | Percent Error Difference Between Desired and Actual |
|---|---|---|
| 50 | 3840 | — |
| 75 | 2560 | — |
| 110 | 1745 | 0.026 |
| 134.5 | 1428 | 0.034 |
| 150 | 1280 | — |
| 300 | 640 | — |
| 600 | 320 | — |
| 1200 | 160 | — |
| 1800 | 107 | — |
| 2000 | 96 | — |
| 2400 | 80 | — |
| 3600 | 53 | 0.628 |
| 4800 | 40 | — |
| 7200 | 27 | 1.23 |
| 9600 | 20 | — |
| 19200 | 10 | — |
| 38400 | 5 | — |
| 56000 | 3 | 14.285 |

### Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in table 2 and are described below.

**Bit 0:** This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 may be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

**Bit 1:** This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

**Bit 2:** This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

**Bit 3:** This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level).

**Bit 4:** This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits).

NOTE

Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

**Bit 5:** This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the WD8250 is ready to accept a new character for transmission. In addition, this bit causes the WD8250 to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

**Bit 6:** This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle. It is reset to logic 0 upon a data transfer from the Transmitter Holding Register to the Transmitter Shift Register. Bit 6 is a read-only bit.

**Bit 7:** This bit is permanently set to logic 0.

### Interrupt Identification Register

The WD8250 has an on chip interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the WD8250 prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and source of that interrupt are stored in the Interrupt Identification Register (refer to table 5). The Interrupt Identification Register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in table 2 and are described below.

**Bit 0:** This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

**Bits 1 and 2:** These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in table 5.

**Bits 3 through 7:** These five bits of the IIR are always logic 0.

### Interrupt Enable Register

This 8-bit register enables the four interrupt sources of the WD8250 to separately activate the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interurpt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in table 2 and are described below.

**Bit 0:** This bit enables the Received Data Available Interrupt when set to logic 1. Bit 0 is reset to logic 0 upon completion of the associated interrupt service routine.

Table 5. Interrupt Control Functions.

| Interrupt Identification Register | | | Interrupt Set and Reset Functions | | | |
|---|---|---|---|---|---|---|
| Bit 2 | Bit 1 | Bit 0 | Priority Level | Interrupt Flag | Interrupt Source | Interrupt Reset Control |
| 0 | 0 | 1 | — | None | None | — |
| 1 | 1 | 0 | Highest | Receiver Line Status | Overrun Error or Parity Error or Framing Error or Break Interrupt | Reading the Line Status Register |
| 1 | 0 | 0 | Second | Received Data Available | Receiver Data Available | Reading the Receiver Buffer Register |
| 0 | 1 | 0 | Third | Transmitter Holding Register Empty | Transmitter Holding Register Empty | Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register |
| 0 | 0 | 0 | Fourth | MODEM Status | Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect | Reading the MODEM Status Register |

**Bit 1:** This bit enables the Receiver Line Status Interrupt when set to logic 1. Bit 2 is reset to logic 0 upon completion of the associated interrupt service routine.

**Bit 3:** This bit enables the MODEM Status Interrupt when set to logic 1. Bit 3 is reset to logic 0 upon completion of the associated interrupt service routine.

**Bits 4 through 7:** These four bits are always logic 0.

**MODEM Control Register**

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in table 2 and are described below.

**Bit 0:** This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

NOTE

The $\overline{DTR}$ output of the WD8250 may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

**Bit 1:** This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

**Bit 2:** This bit controls the Output 1 ($\overline{OUT\ 1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described above for bit 0.

**Bit 3:** This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described above for bit 0.

**Bit 4:** This bit provides a loopback feature for diagnostic testing of the WD8250. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) are disconnected; and the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four MODEM Control inputs. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the WD8250.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The WD8250 interrupt system can be tested by writing into the lower six bits of the Line Status Register

and the lower four bits of the MODEM Status Register. Setting any of these bits to a logic 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal WD8250 operation. To return to this operation, the registers must be reprogrammed for normal operation and then bit 4 must be reset to logic 0.

**Bits 5 through 7:** These bits are permanently set to logic 0.

**MODEM Status Register**

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in table 2 and are described below.

**Bit 0:** This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

**Bit 1:** This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

**Bit 2:** This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from an On (logic 1) to an Off (logic 0) condition.

**Bit 3:** This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the $\overline{RLSD}$ input to the chip has changed state.

NOTE

Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

**Bit 4:** This bit is the complement of the Clear to Send ($\overline{CTS}$) input.

**Bit 5:** This bit is the complement of the Data Set Ready ($\overline{DSR}$) input.

**Bit 6:** This bit is the complement of the Ring Indicator ($\overline{RI}$) input.

**Bit 7:** This bit is the complement of the Received Line Signal Detect ($\overline{RLSD}$) input.

**Typical Applications**

Figures 1 and 2 show how to use the WD8250 chip in an 8080A system and in a microcomputer system with a high-capacity data bus.

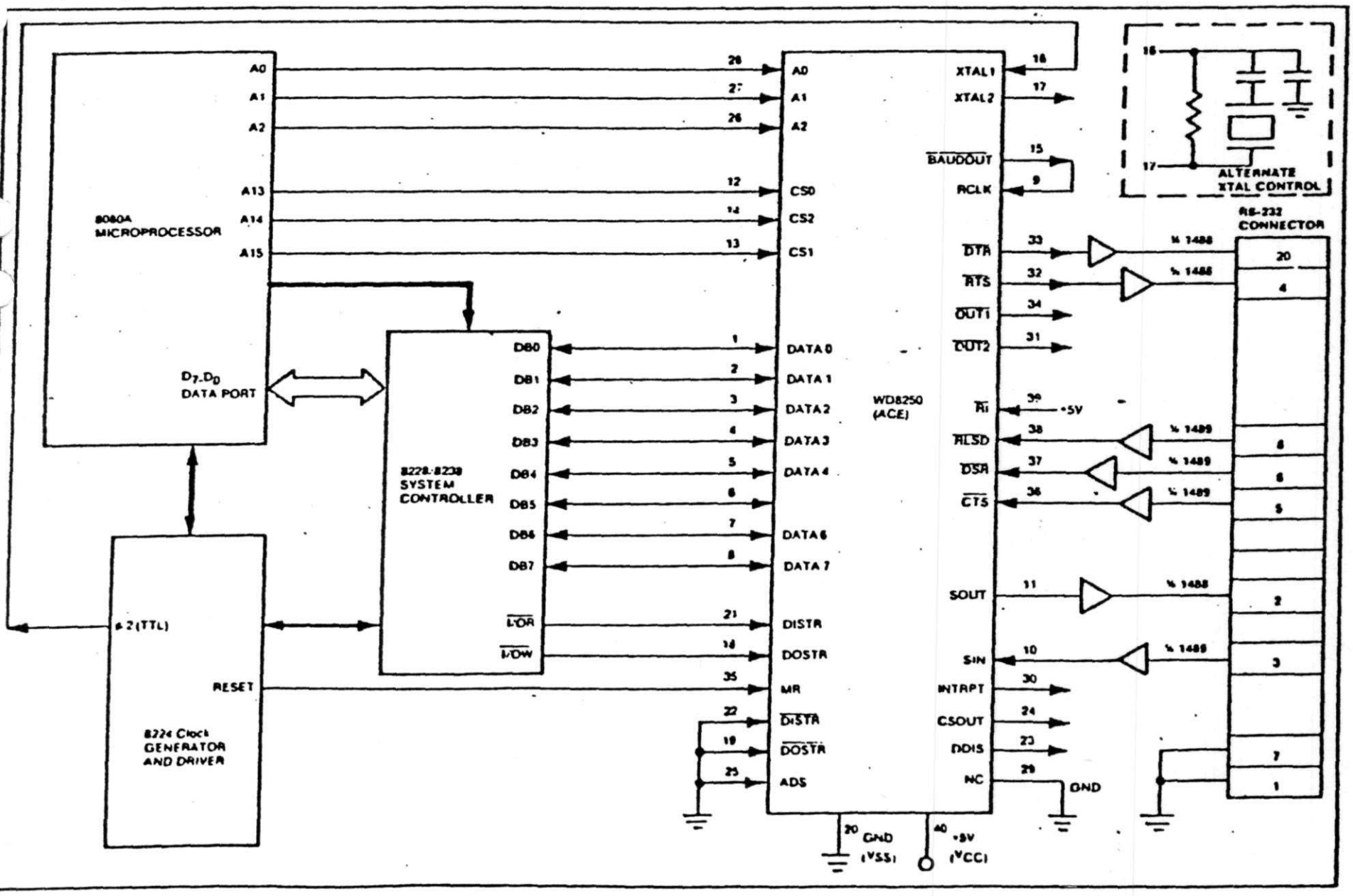



FIGURE 1. TYPICAL 8-BIT MICROPROCESSOR/RS-232 TERMINAL INTERFACE USING THE ACE.

## Typical Applications (continued)

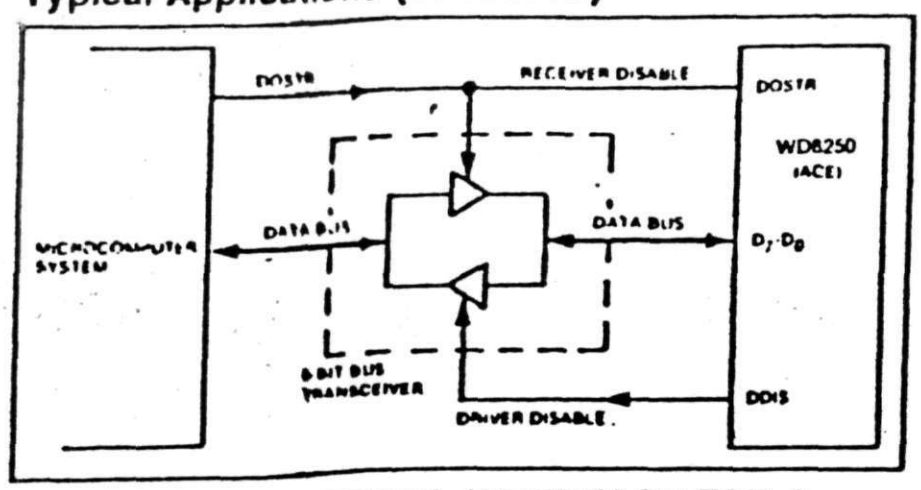



**FIGURE 2. TYPICAL INTERFACE FOR A HIGH-CAPACITY DATA BUS.**

## ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... 0°C to +70°C
Storage Temperature -65°C to +150°C (Ceramic)
-50°C to +125°C (Plastic)
All Input or Output Voltages with
Respect to $V_{SS}$ ..... -0.5 V to +7.0 V
Power Dissipation ..... 400 mW

***Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.***

## DC Electrical Characteristics

$T_A$ = 0°C to +70°C, $V_{CC}$ = +5V ± 5%, $V_{SS}$ = 0V, unless otherwise specified.

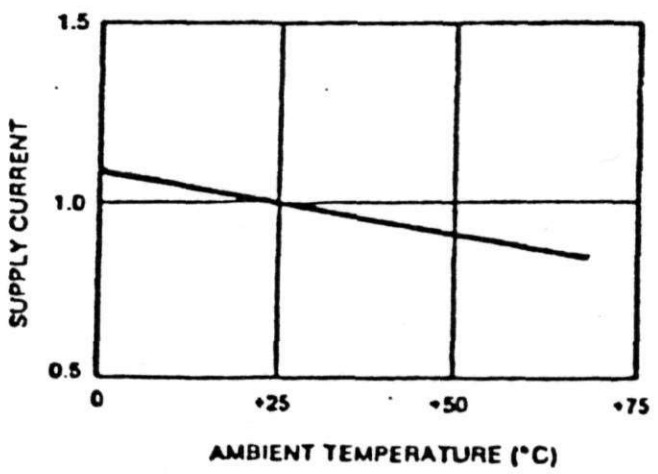
| Symbol | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{ILX}$ | Clock Input Low Voltage | -0.5 | | 0.8 | V | |
| $V_{IHX}$ | Clock Input High Voltage | 2.0 | | $V_{CC}$ | V | |
| $V_{IL}$ | Input Low Voltage | -0.5 | | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | 2.0 | | $V_{CC}$ | V | |
| $V_{OL}$ | Output Low Voltage | | | 0.4 | V | $I_{OL}$=1.6mA on all outputs |
| $V_{OH}$ | Output High Voltage | 2.4 | | | V | $I_{OH}$=-100 µA |
| $I_{CC(AV)}$ | Avg Power Supply Current ($V_{CC}$) | | 65 | 80 | ma | |
| $I_{IL}$ | Input Leakage | | | ± 10 | µA | |
| $I_{CL}$ | Clock Leakage | | | ± 10 | µA | |

### Capacitance

$T_A$ = 25°C, $V_{CC}$ = $V_{SS}$ = 0V

| Symbol | Parameter | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|
| $C_{XIN}$ | Clock Capacitance | 10 | 15 | pF | fc=1 MHz Unmeasured pins returned to $V_{SS}$ |
| $C_{IN}$ | Input Capacitance | 6 | 10 | pF | |
| $C_{OUT}$ | Output Capacitance | 10 | 20 | pF | |

Typical Supply Current vs. Temperature, Normalized

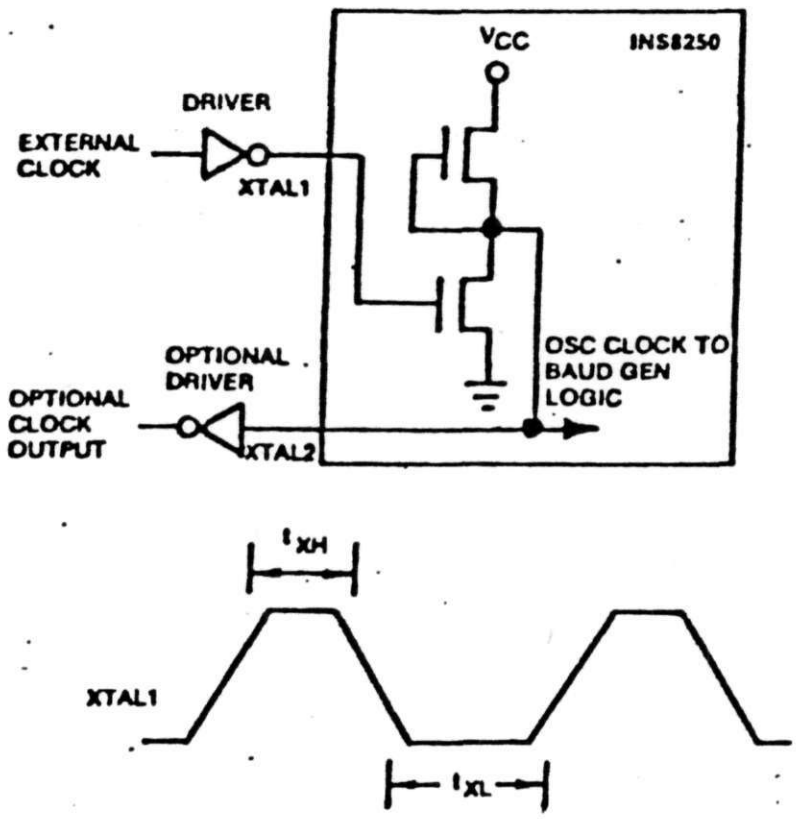


AC Electrical Characteristic $T_A$ = 0°C to +70°C, $V_{CC}$ = +5V ± 5%

| Symbol | Parameter | Typical | Units | Test Conditions |
|---|---|---|---|---|
| $t_{AW}$ | Address Strobe Width | 100 | ns | |
| $t_{AS}$ | Address Setup Time | 110 | ns | |
| $t_{AH}$ | Address Hold Time | 10 | ns | |
| $t_{CSS}$ | Chip Select Output Delay from Strobe | 100 | ns | |
| $t_{DID}$ | $\overline{DISTR}$/DISTR Strobe Delay | 100 | ns | |
| $t_{DIW}$ | $\overline{DISTR}$/DISTR Strobe Width | 200 | ns | |
| $t_{RC}$ | Read Cycle Delay | 2000 | ns | |
| RC | Read Cycle=$t_{AW}$ + $t_{DID}$ + $t_{DIW}$ + $t_{RC}$ | 2400 | ns | |
| $t_{DD}$ | $\overline{DISTR}$/DISTR to Driver Disable Delay | 150 | ns | |
| $t_{DDD}$ | Delay from $\overline{DISTR}$/DISTR to Data | 250 | ns | |
| $t_{HZ}$ | $\overline{DISTR}$/DISTR to Floating Data Delay | 100 | ns | |
| $t_{DOD}$ | $\overline{DOSTR}$/DOSTR Strobe Delay | 200 | ns | |
| $t_{DOW}$ | $\overline{DOSTR}$/DOSTR Strobe Width | 200 | ns | |
| $t_{WC}$ | Write Cycle Delay | 2000 | ns | |
| WC | Write Cycle=$t_{AW}$ + $t_{DOD}$ + $t_{DOW}$ + $t_{WC}$ | 2500 | ns | |
| $t_{DS}$ | Data Setup Time | 200 | ns | |
| $t_{DH}$ | Data Hold Time | 50 | ns | |
| $t_{CSC}$ | Chip Select Output Delay from Select | 200 | ns | |
| $t_{DIC}$ | $\overline{DISTR}$/DISTR Delay from Select | 200 | ns | |
| $t_{DOC}$* | $\overline{DOSTR}$/DOSTR Delay from Select | 200 | ns | |

*Applicable only when $\overline{ADS}$ input is not tied permanently low.

| Symbol | Parameter | Min. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|
| **Baud Generator** | | | | | |
| N | Baud Rate Divisor | 1 | $2^{16}-1$ | | |
| $t_{BLD}$ | Baud Output Negative Edge Delay | | 250 typ | ns | 100pF Load |
| $t_{BHD}$ | Baud Output Positive Edge Delay | | 250 typ | ns | 100pF Load |
| $t_{LW}$ | Baud Output Down Time | 425 typ | | ns | 100pF Load |
| $t_{HW}$ | Baud Output Up Time | 330 Typ | | ns | 100pF Load |
| **Receiver** | | | | | |
| $t_{SCD}$ | Delay from RCLK to Sample Time | | 2 typ | μs | |
| $t_{SINT}$ | Delay from Stop to Set Interrupt | | 2 typ | μs | 100pF Load |
| $t_{RINT}$ | Delay from $\overline{DISTR}$/DISTR (RD RBR) to Reset Interrupt | | 1 typ | μs | 100pF Load |
| **Transmitter** | | | | | |
| $t_{HR}$ | Delay from $\overline{DOSTR}$/DOSTR (WR THR) to Reset Interrupt | | 1 typ | μs | 100pF Load |
| $t_{IRS}$ | Delay from Initial INTR Reset to Transmit Start | | 16 typ | $\overline{BAUDOUT}$ Cycles | |
| $t_{SI}$ | Delay from Initial Write to Interrupt | | 24 typ | $\overline{BAUDOUT}$ Cycles | |
| $t_{SS}$ | Delay from Stop to Next Start | | 1 typ | μs | |
| $t_{STI}$ | Delay from Stop to Interrupt (THRE) | | 8 typ | $\overline{BAUDOUT}$ Cycles | |
| TIR | Delay from $\overline{DISTR}$/DISTR (RD IIR) to Reset Interrupt (THRE) | | 1 typ | μs | 100pF Load |
| **Modem Control** | | | | | |
| $t_{MDO}$ | Delay from DOSTR/$\overline{DOSTR}$ (WR MCR) to Output | | 1 typ | μs | 100pF Load |
| $t_{SIM}$ | Delay to Set Interrupt from MODEM Input | | 1 typ | μs | 100pF Load |
| $t_{RIM}$ | Delay to Reset Interrupt from $\overline{DISTR}$/DISTR (RD MSR) | | 1 typ | μs | 100pF Load |

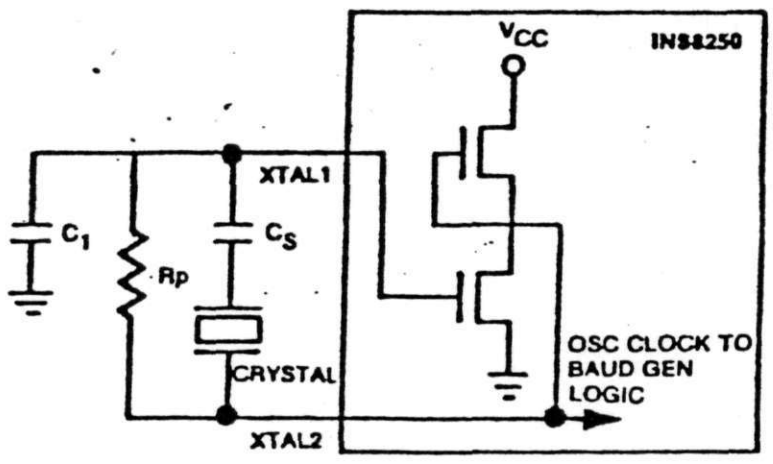






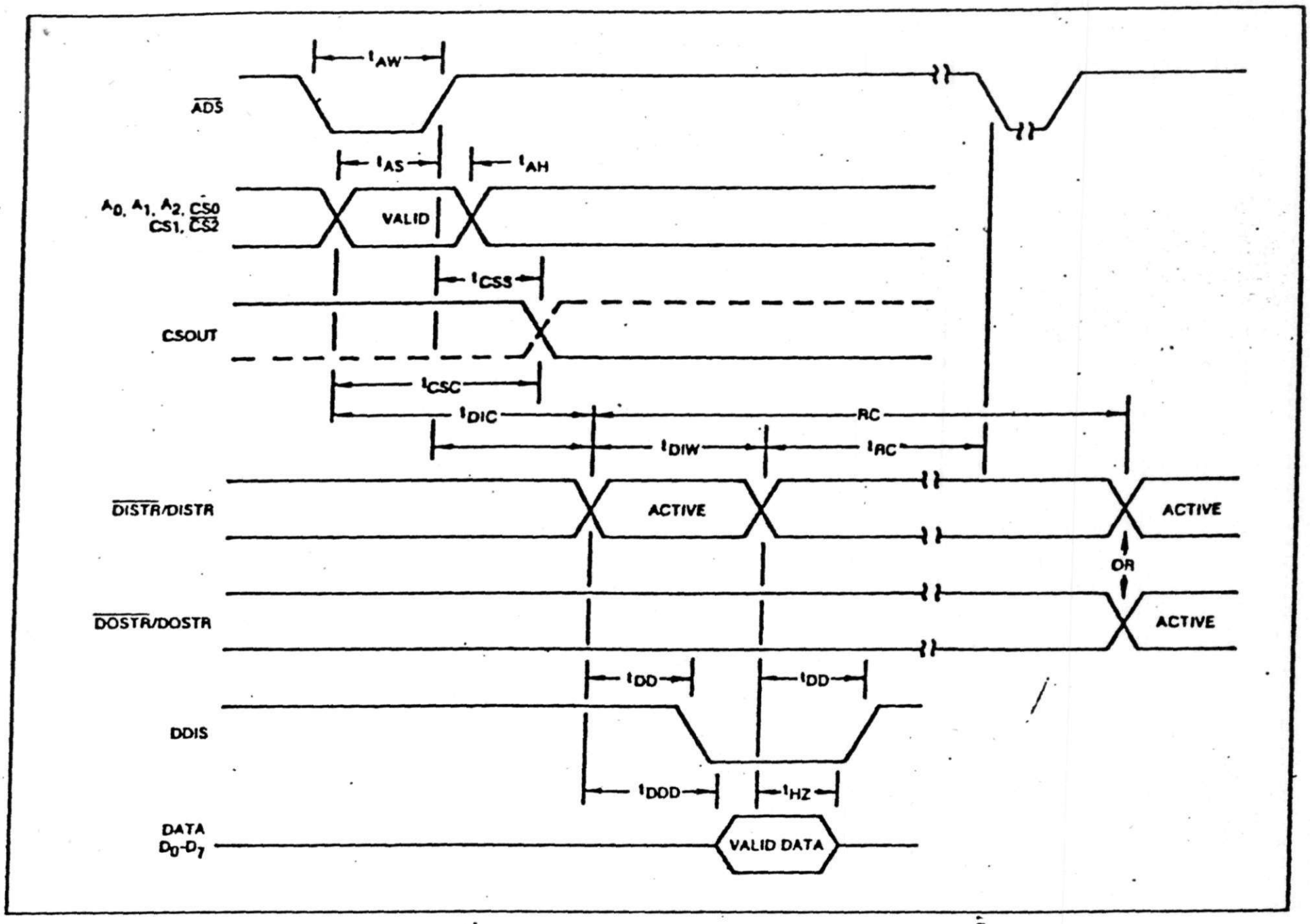
| Timing | Min | Units |
|---|---|---|
| tXH | 100 | ns |
| tXL | 115 | ns |

**EXTERNAL CLOCK INPUT (3.1 MHz MAX.)**

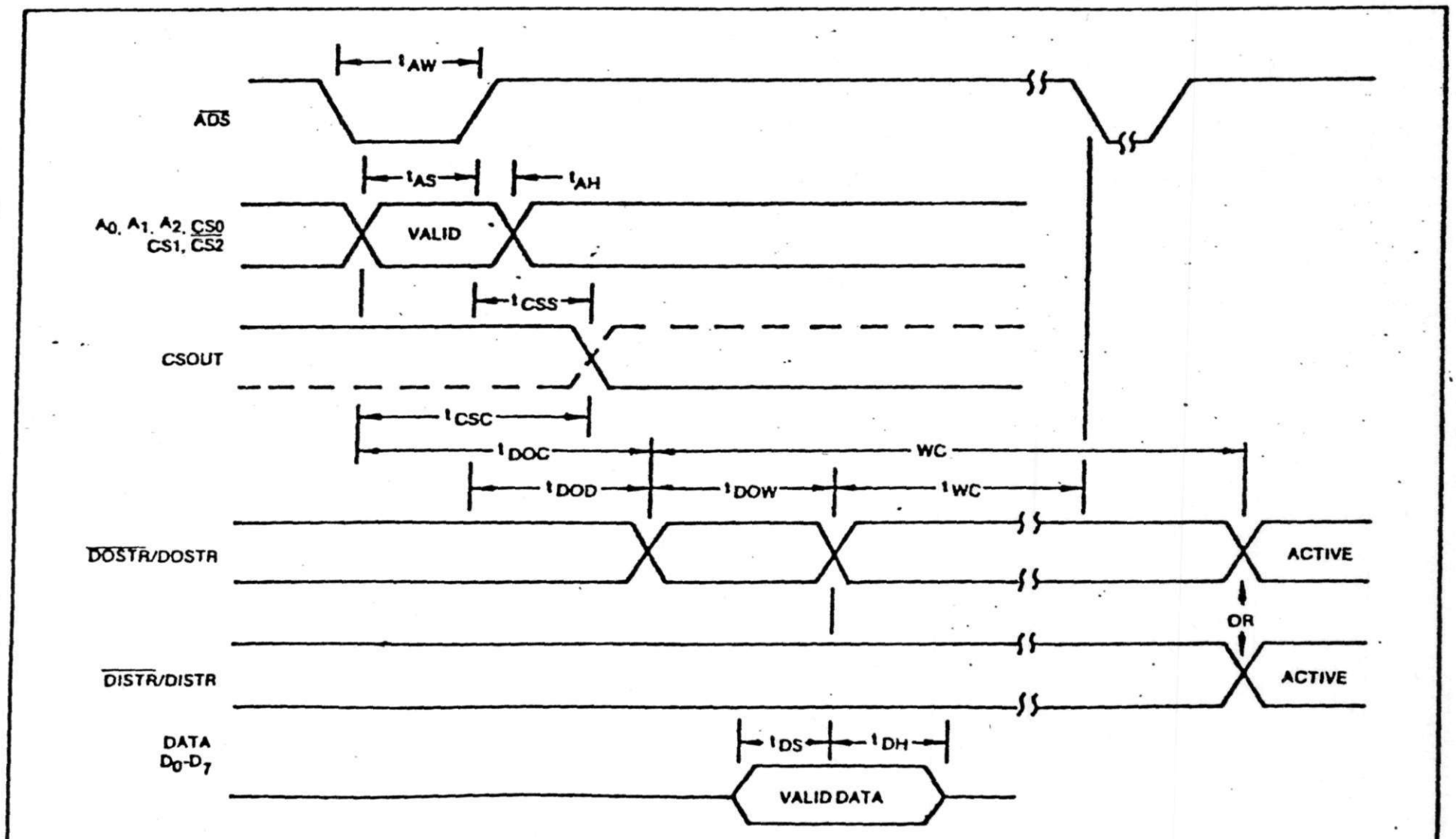



| CRYSTAL | Rp | CS | C1 |
|---|---|---|---|
| 3.1 MHz | 1 MΩ | 50 pF | 10 pF |

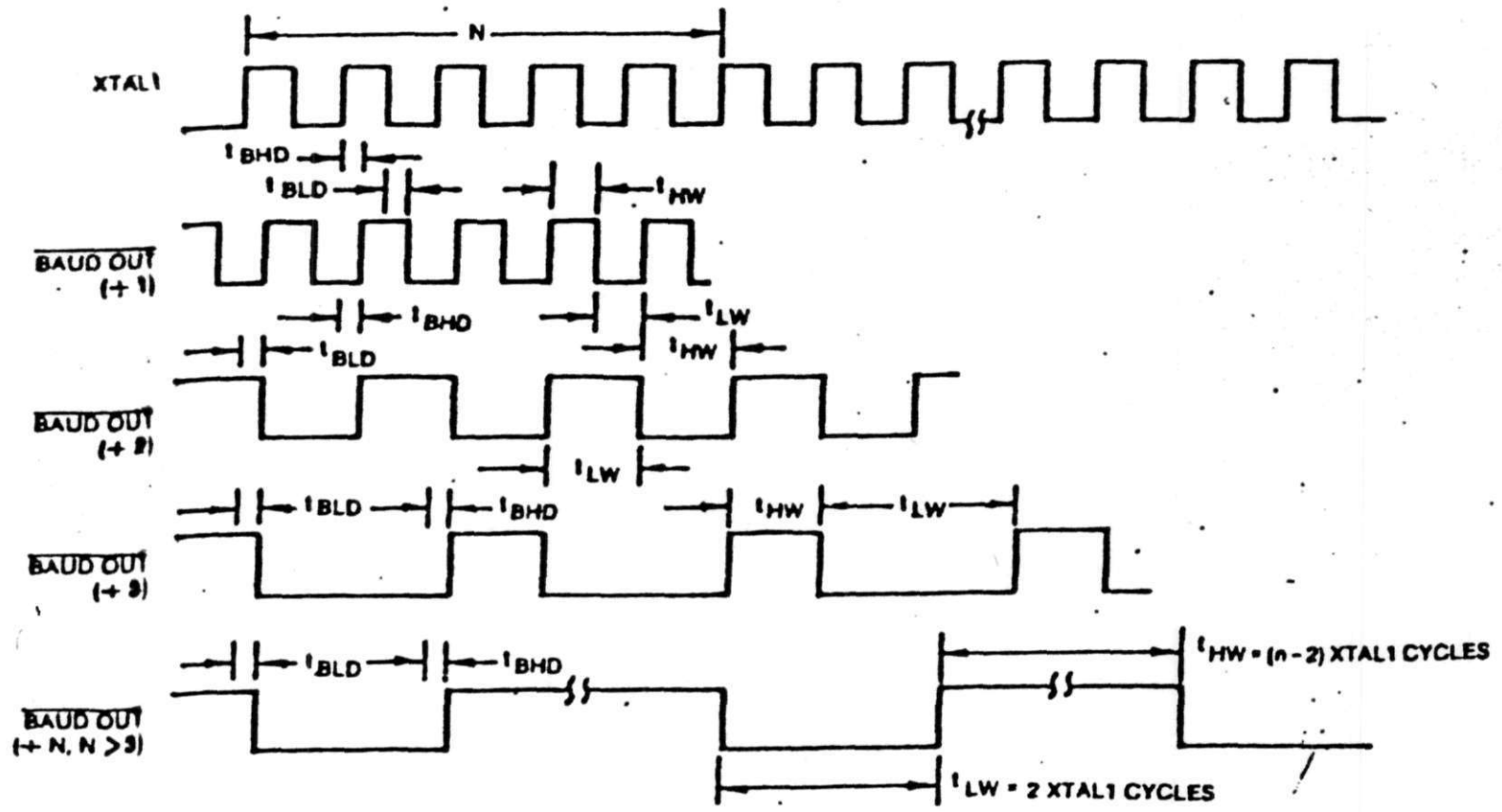
**TYPICAL CRYSTAL OSCILLATOR NETWORK**



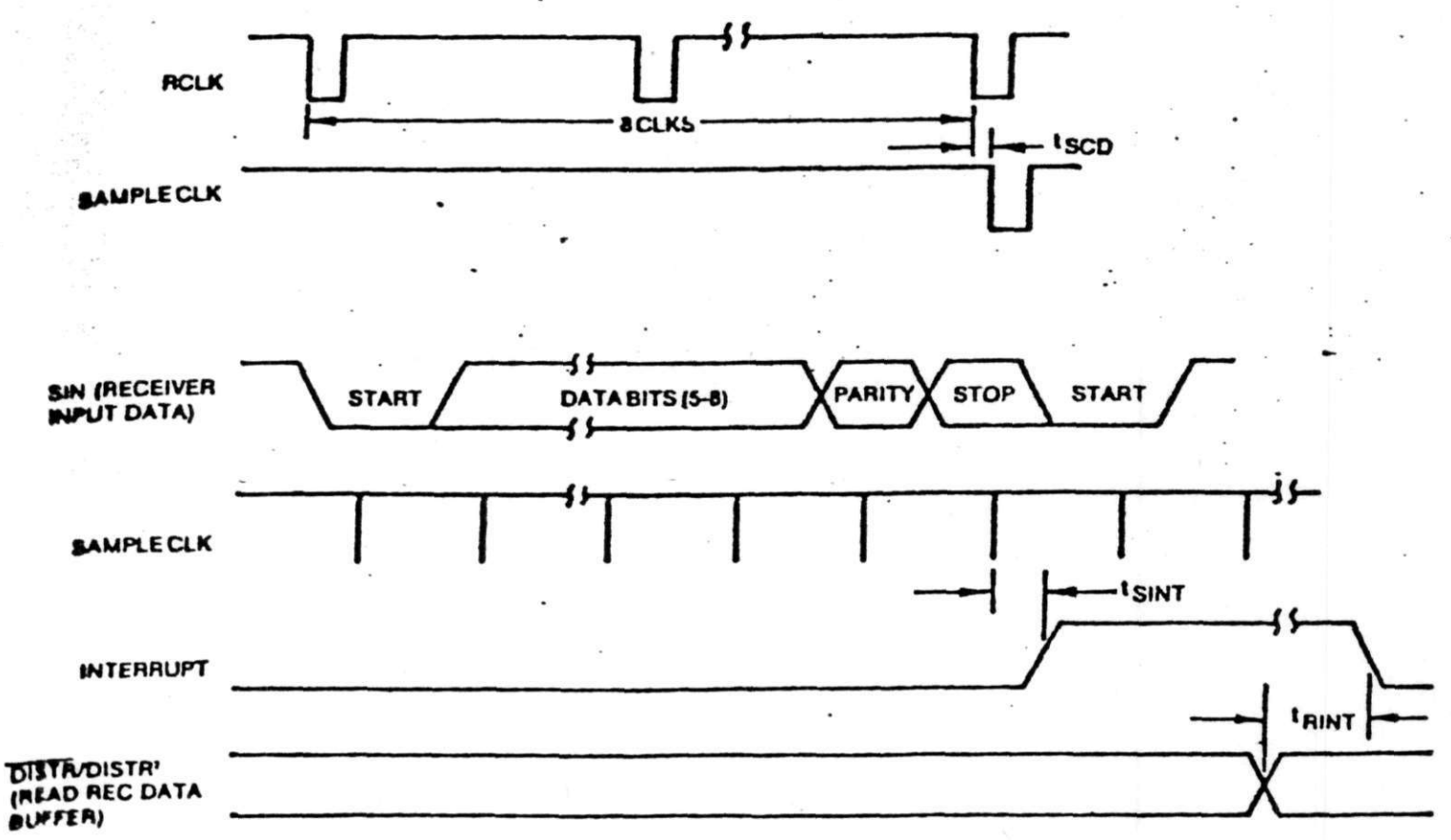

READ CYCLE TIMING




WRITE CYCLE TIMING

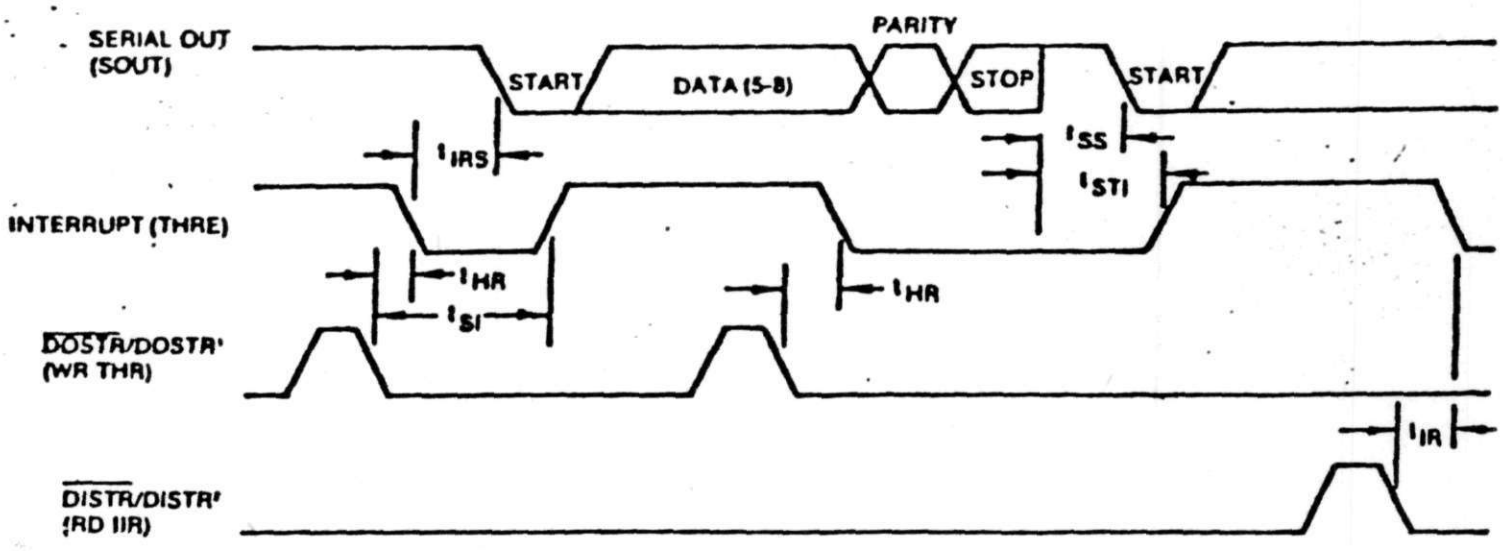



**BAUDOUT TIMING**



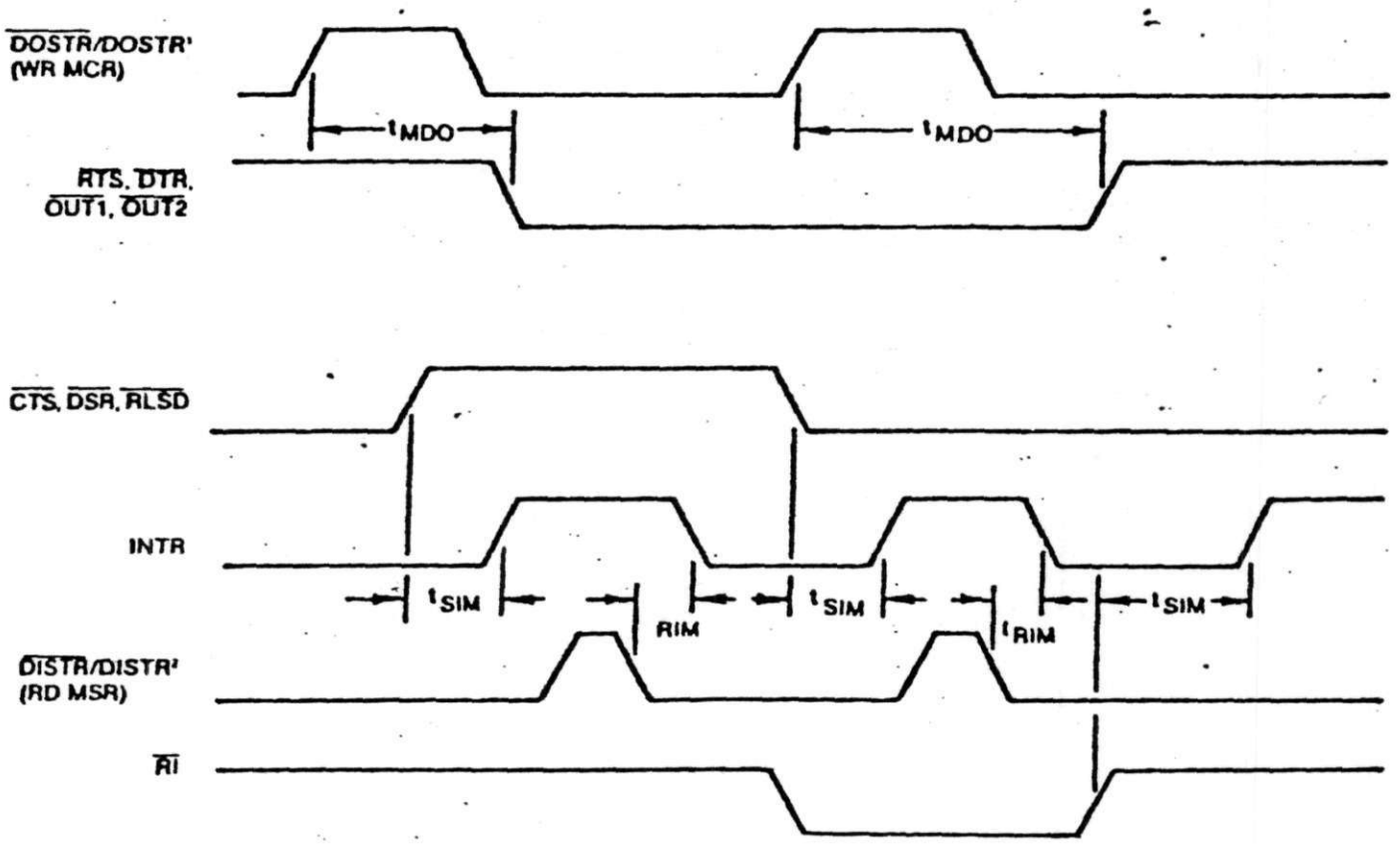

Notes:
tWC See Write Cycle Timing
tRC See Read Cycle Timing

**RECEIVER TIMING**



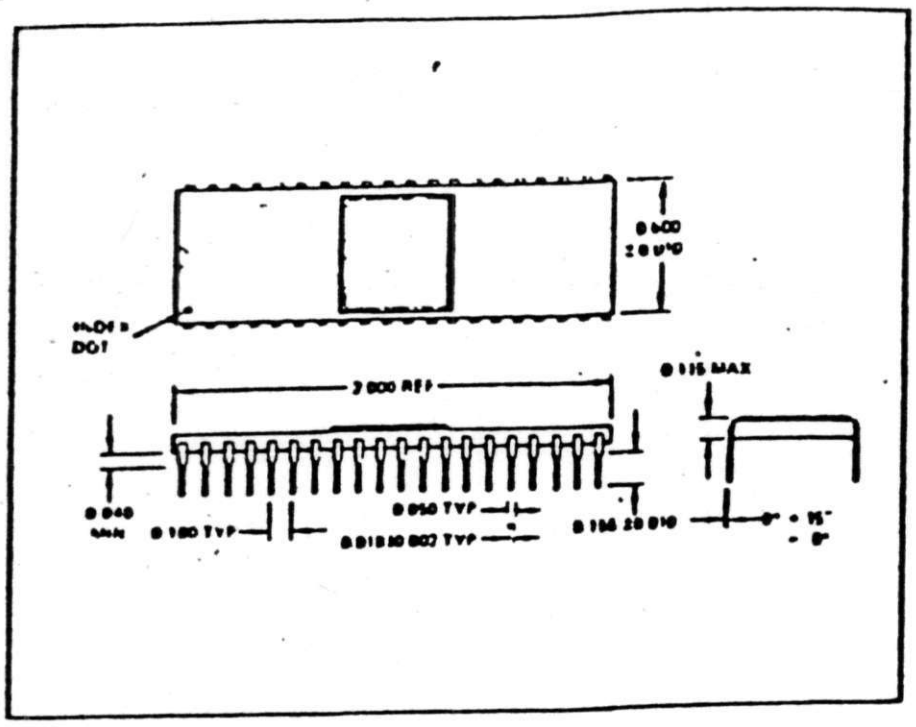

Notes:
¹See Write Cycle Timing
²See Read Cycle Timing

**TRANSMITTER TIMING**

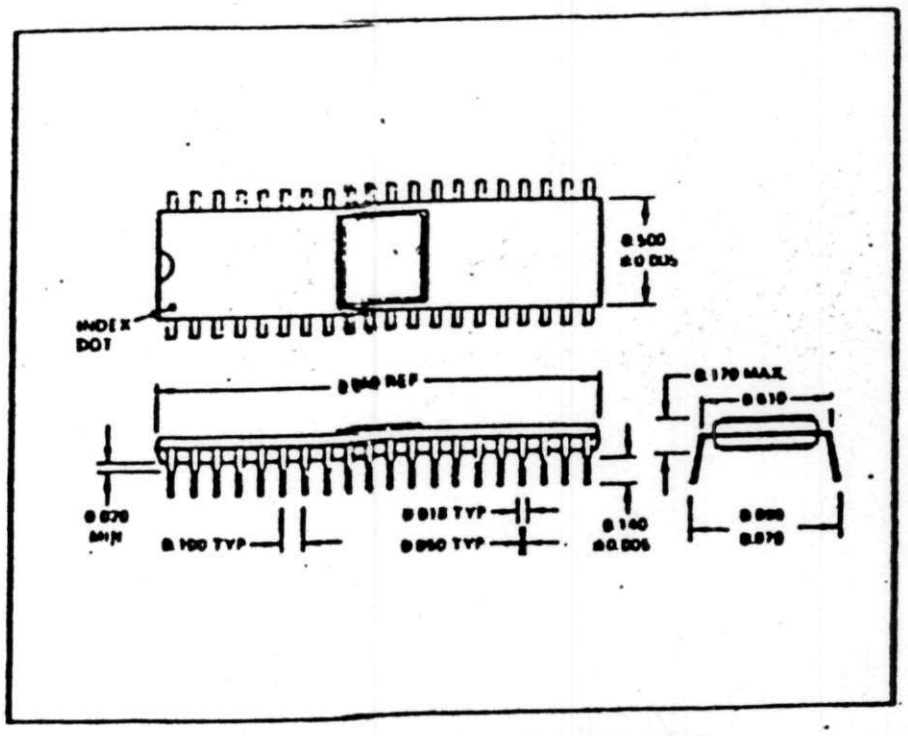



Notes:
¹See Write Cycle Timing
²See Read Cycle Timing

**MODEM CONTROLS TIMING**



WD8250 CERAMIC PACKAGE



WD8250 PLASTIC PACKAGE

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.



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